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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,738	10/15/2003	Kyung-Soo Kim	SAM-0465	6148

7590

06/20/2006

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EXAMINER

CHEN, KIN CHAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,738

Applicant(s)

KIM ET AL.

Examiner

Kin-Chan Chen

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2006.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 10-18 and 21 is/are allowed.
6) ☒ Claim(s) 1-9, 19, 20 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. **The claim(s) contains subject matter which was not described in the specification** in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 19, "forming a fourth dielectric layer using a different material from that of the second dielectric layer, on the second dielectric layer" is new matter. "remove a portion of the fourth dielectric layer so as to selectively expose a portion of the second dielectric layer" is new matter.

In claim 20, "forming gate electrodes on the gate dielectric layers of the thick portion and the thin portion respectively" is new matter.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6, and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Chern et al. (US 2003/0102504).

It is noted that applicant states "the gate dielectric layer" which may be applied for forming gate electrode. Because **it is for the intended use**, it has not been given patentable weight. In light of the applicant's specification (e.g., page 6, lines 28-30; page 8, line 5), gate dielectric materials may be silicon oxide or silicon nitride.

In a method for forming multiple thickness dielectric layers (such as oxide or nitride, so-called gate dielectric layers in instant claims) , Chern (Figs 3c and 3d; [0021]-[0022]) teaches that a dielectric may be formed on a semiconductor substrate. A portion of dielectric layer may be removed so as to expose a portion of the dielectric layer to form a gate dielectric layer including a thick portion of the dielectric layer and a thin portion formed of the exposed dielectric layer. The thin portion being of the first thickness and the thick portion being of a combined thickness of the first thickness and the second thickness. The dielectric materials may be oxide or nitride. The first dielectric layer may be formed of thermal oxide through rapid thermal oxidation. The etching may be dry or wet etching. Since the second dielectric is etched and the first layer remains, therefore the etch rate of the second dielectric layer is higher than that of the first dielectric.

4. Claims 1, 2, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 2002/0119615).

It is noted that applicant states "the gate dielectric layer" which may be applied for forming gate electrode. Because it is for the intended use, it has not been given patentable weight. In light of the applicant's specification (e.g., page 6, lines 28-30; page 8, line 5), gate dielectric materials may be silicon oxide or silicon nitride.

In a method for forming multiple thickness dielectric layers (such as oxide or nitride, so-called gate dielectric layers in instant claims), Kim (**Figs 13-15**; [0057]-[0058]) teaches that a dielectric may be formed on a semiconductor substrate. A portion of dielectric layer may be removed so as to expose a portion of the dielectric layer to form a gate dielectric layer including a thick portion of the dielectric layer and a thin portion formed of the exposed dielectric layer. The thin portion being of the first thickness and the thick portion being of a combined thickness of the first thickness and the second thickness. The dielectric materials may be oxide or nitride.

The etching may be dry or wet etching. Since the second dielectric is etched and the first layer remains, therefore the etch rate of the second dielectric layer is higher than that of the first dielectric.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claim 5, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern et al. (US 2003/0102504).

In a method for forming multiple thickness gate dielectric layers, Chern (Figs 3c and 3d; [0021]-[0022]) teaches that a dielectric may be formed on a semiconductor substrate. A portion of dielectric layer may be removed so as to expose a portion of the dielectric layer to form a gate dielectric layer including a thick portion of the dielectric layer and a thin portion formed of the exposed dielectric layer. The thin portion being of the first thickness and the thick portion being of a combined thickness of the first thickness and the second thickness. The dielectric materials may be oxide or nitride. The first dielectric layer may be formed of thermal oxide through rapid thermal oxidation. The etching may be dry or wet etching. Since the second dielectric is etched and the first layer remains, therefore the etch rate of the second dielectric layer is higher than that of the first dielectric.

Dependent claim 9 differs from Chern by repeating the process by using three dielectric layers. It would have been obvious to one with ordinary skill in the art to use the combination of three dielectric layers because they have been used for the same purpose as gate dielectric, and repeat the foregoing process steps.

The above-cited claims differ from Chern by specifying well-known features (such as using hafnium oxide or aluminum oxide in claim 5; nitridizing the surface of dielectric layer in claim 8) to the art of semiconductor device fabrication. A person having ordinary skill in the art would have found it obvious to modify Chern by adding any of same well-known features to same in order to meet specific product design and

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requirement with a reasonable expectation of success. The examiner takes official notice of facts that applicant did not traverse the aforementioned conventionality (e.g., well-known features, common knowledge), which have been stated in the previous office action (May 10, 2005).

Response to Arguments

7. Applicant has argued that the prior art does not teach so-called the gate dielectric layer. It is not persuasive. As has been stated in the office action, the gate dielectric layer" which may be applied for forming gate electrode. Because it is for the intended use, it has not been given patentable weight. In light of the applicant's specification (e.g., page 6, lines 28-30; page 8, line 5), gate dielectric material may be silicon oxide or silicon nitride, which is same as the material disclosed by Chern or Kim.

Applicant has argued that the nitride layer of Chern is then removed, so it is not considered gate dielectric layer. It is not persuasive. Chern's process **comprises** the process steps set forth in the instant claims. Same reasoning applies to Kim.

Allowable Subject Matter

8. Claims 10-18 and 21 are allowed.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

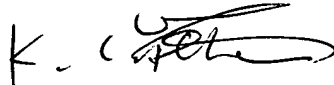
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (571) 272-1461. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 15, 2006


Kin-Chan Chen
Primary Examiner
Art Unit 1765

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